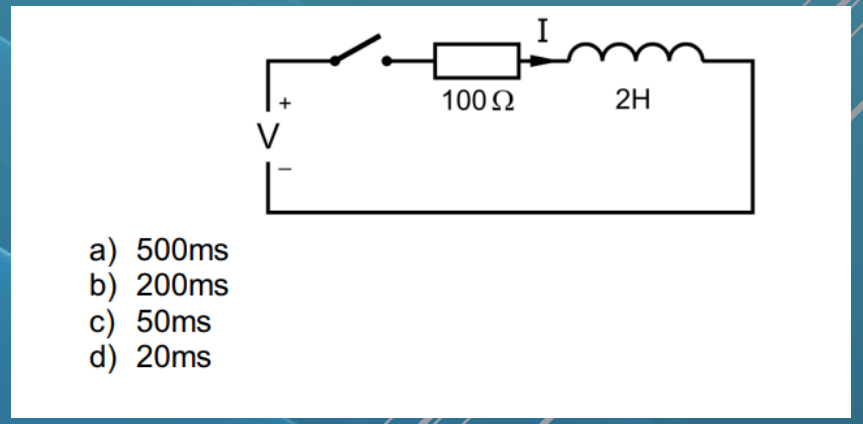
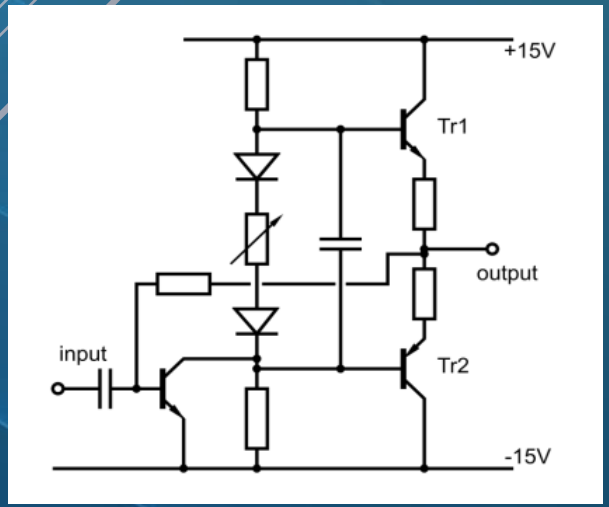


a) 500ms
b) 200ms
c) 50ms
d) 20ms

QUESTION OF THE WEEK

The Amateur Exam Explained : Potential Dividers



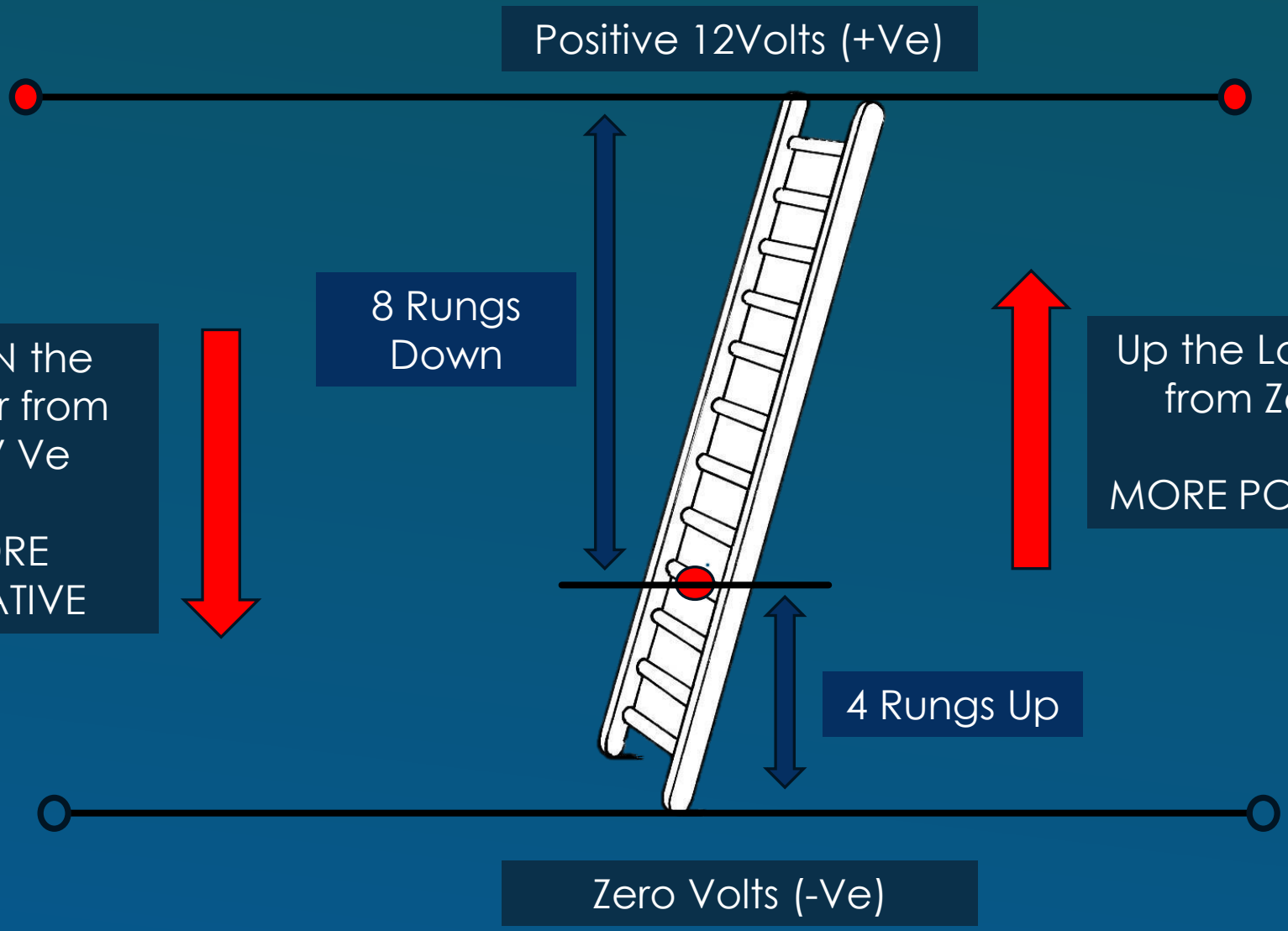
Max Townend G4SDX
Halifax & District ARS

WHAT IS A POTENTIAL DIVIDER?

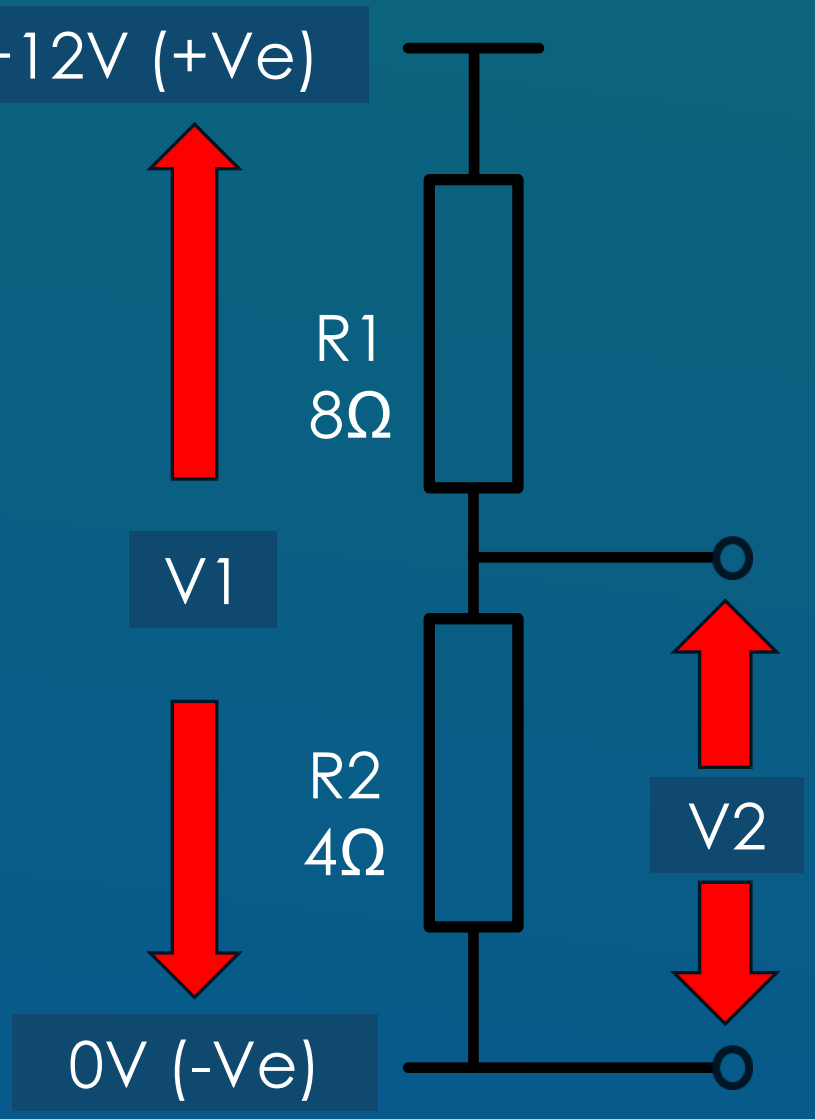
I need the RATIO of the Rungs

4 / 8 + 4

4 / 12 = 1/3



A ‘REAL WORLD’ POTENTIAL DIVIDER ..



$$V2 = (R2 / R1 + R2) \times V1$$

Plug in the NUMBERS

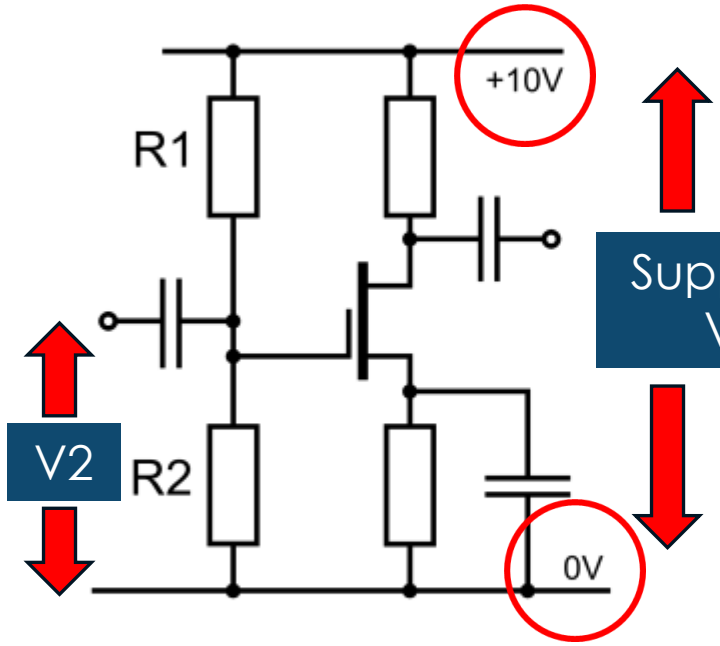
$$V2 = (4 / 8 + 4) \times 12V$$
$$V2 = 4 /12 \times 12V$$
$$V2 = 1/3 \times 12V$$
$$\underline{V2 = 4V}$$

NO COMPONENT IS PERFECT – IT HAS 'TOLERANCE'

COLOR	FIRST AND SECOND BANDS SIGNIFICANT DIGITS	THIRD BAND MULTIPLIER	FOURTH BAND TOLERANCE
BLACK	0	10^0	
BROWN	1	10^1	1%
RED	2	10^2	2%
ORANGE	3	10^3	3%
YELLOW	4	10^4	4%
GREEN	5	10^5	
BLUE	6	10^6	
VIOLET	7	10^7	
GRAY	8	10^8	
WHITE	9	10^9	
GOLD	-	10^{-1}	5%
SILVER	-	10^{-2}	10%
NONE	-		20%

HAVE WE UNDERSTOOD THE QUESTION?

The drawing shows an FET circuit biased by R1 and R2. R1 is 80kΩ and R2 is 20kΩ. Both resistors are 10% tolerance. The bias voltage might be lower than its design value by a maximum of



A. 180mV
B. 100mV
C. 300mV
D. 200mV.

The Value of R1 = 80K
The Value of R2 = 20K

Supply voltage V1 is 10V

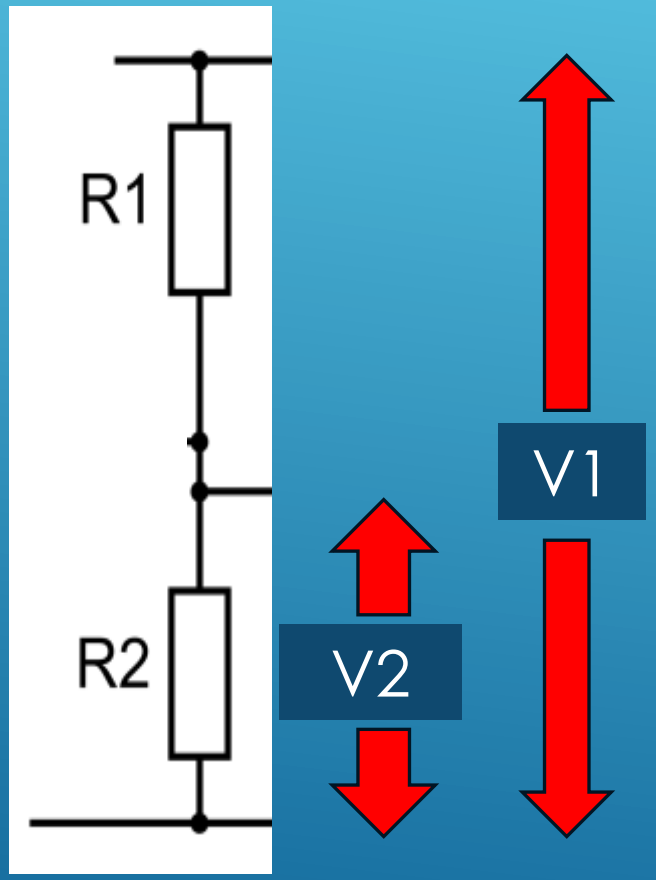
The TOLERANCE of R1 and R2 is +/- 10%

$$V2 = R2/R1+R2 \times V1$$

The first thing to notice about this question is the level of irrelevant 'Clutter' that has been introduced by the examiner. FOCUS ON WHAT IS BEING ASKED!

This is A SIMPLE question about a POTENTIAL DIVIDER and what happens to the VOLTAGE if the value of the resistors are affected by the MANUFACTURING TOLERANCE

SIMPLIFY THE DIAGRAM AND THE PROBLEM



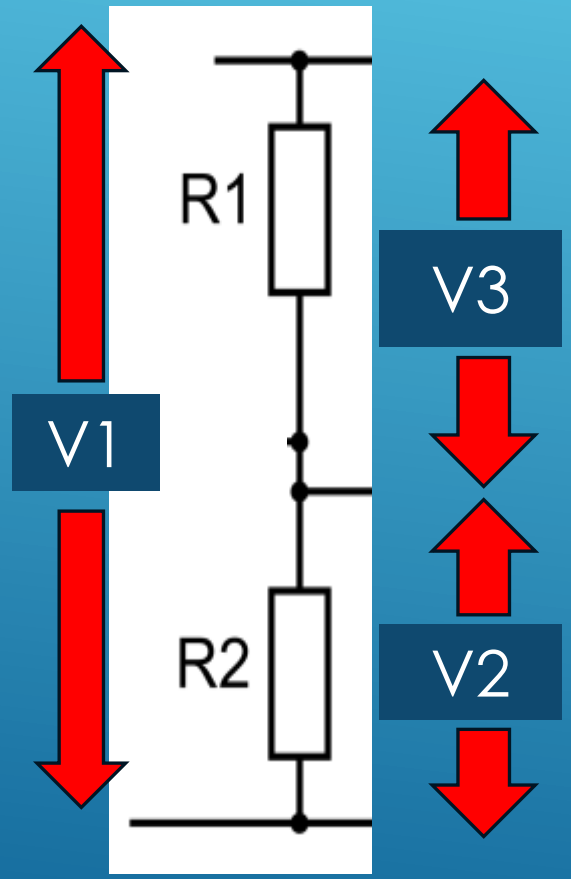
Start by assuming the resistors are PERFECT and EXACTLY the value the designer intended

Make sure the RESISTOR VALUES are all specified in the SAME UNITS – Ohm, KΩ, MΩ, etc. It is the RATIO of the Values we need, and ONLY the RATIO

Plug in the NUMBERS

$$V2 = 20K/20K+ 80K \times 10$$
$$V2 = 20/100 \times 10$$
$$V2 = 0.2 \times 10$$
$$V2 = 2V$$

TOLERANCE AND THE POTENTIAL DIVIDER..



Understand that in a POTENTIAL DIVIDER, if R1 goes UP, V3 goes UP and V2 goes DOWN – It balances like a SEE-SAW

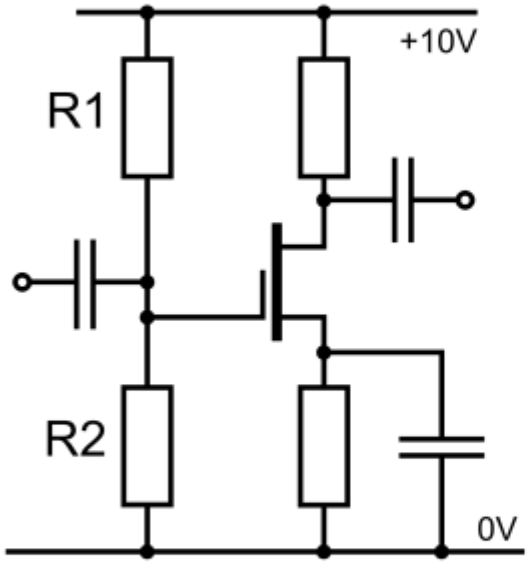
The WORST CASE for the Designer would be if R1 went UP by its MAXIMUM TOLERANCE and R2 went DOWN by its MAXIMUM TOLERANCE (remember the QUESTION)

Worst Case for R1 Would be 80K + 10% = 88KΩ
Worst Case for R2 Would be 20K – 10% = 18KΩ

V2 = 18K/88K+18K x 10
V2 = 18/106 x 10
V2 = 0.17 x 10
V2 = 1.7V (Was 2.0V)
V2 Has DROPPED by 0.3V (300mV)

BACK TO THE QUESTION…..

The drawing shows an FET circuit biased by R1 and R2. R1 is 80kΩ and R2 is 20kΩ. Both resistors are 10% tolerance. The bias voltage might be lower than its design value by a maximum of



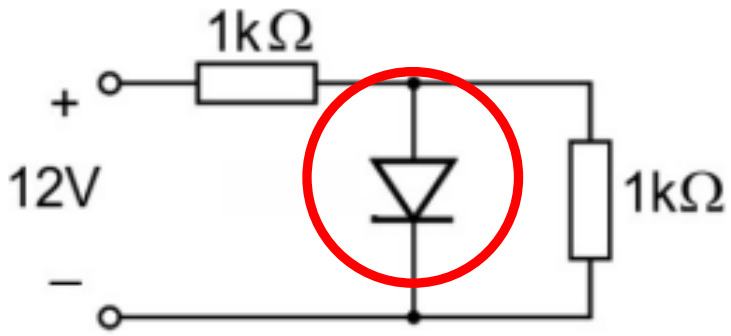
A. 180mV
B. 100mV
C. 300mV
D. 200mV.

Worst Case for R1 Would be 80K + 10% = 88KΩ
Worst Case for R2 Would be 20K – 10% = 18KΩ

The Bias V2 Was DESIGNED to be 2.0V
V2 Has DROPPED to 1.7V (by 300mV) because of MANUFACTURING TOLERANCE in R1 and R2.

A LITTLE PUZZLER FOR YOU ….

26. What current is flowing through the diode shown in the diagram?



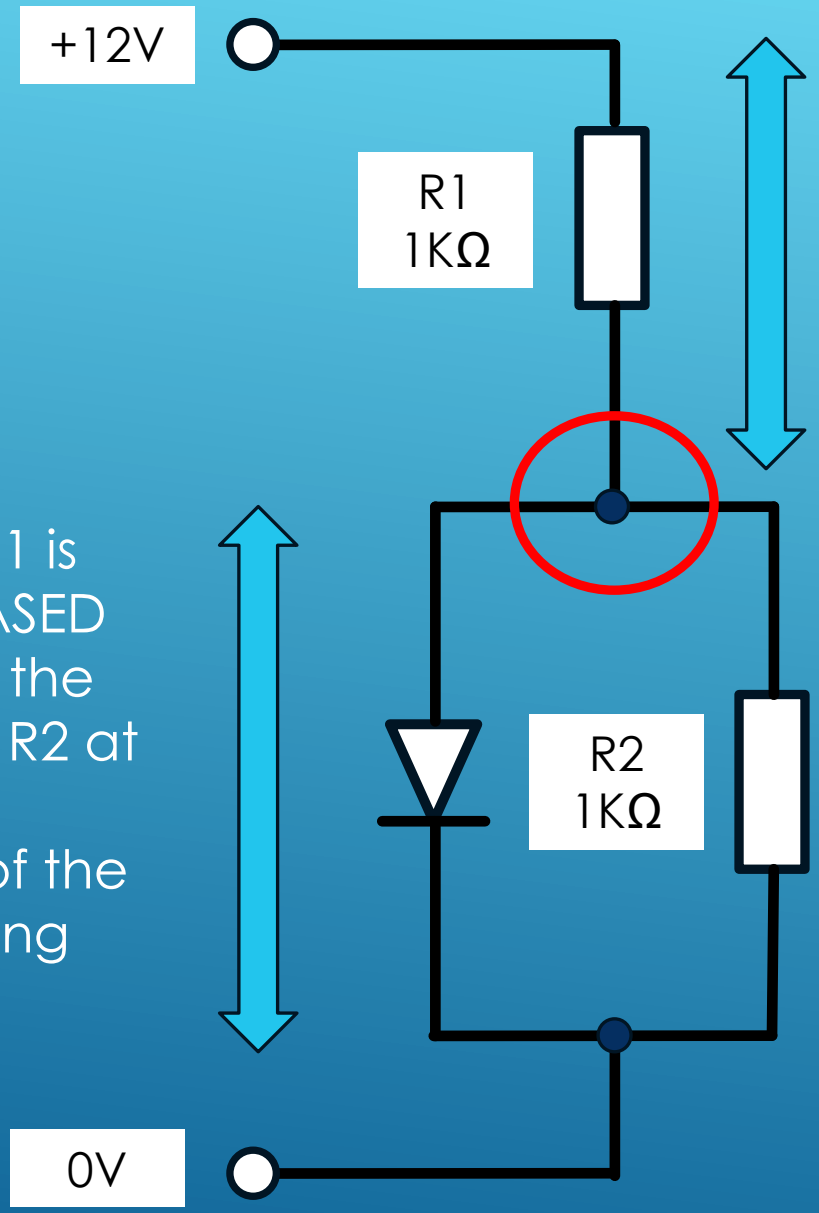
A. 11.3mA.
B. 4.8mA.
C. 0mA.
D. 10.6mA.

Note!
We CANNOT solve this problem using Ohm's Law alone.

There is a NON-LINEAR device in the circuit in the form of a Semiconductor Junction

We must first establish if it is FORWARD or REVERSE BIAS.

STEP 1….



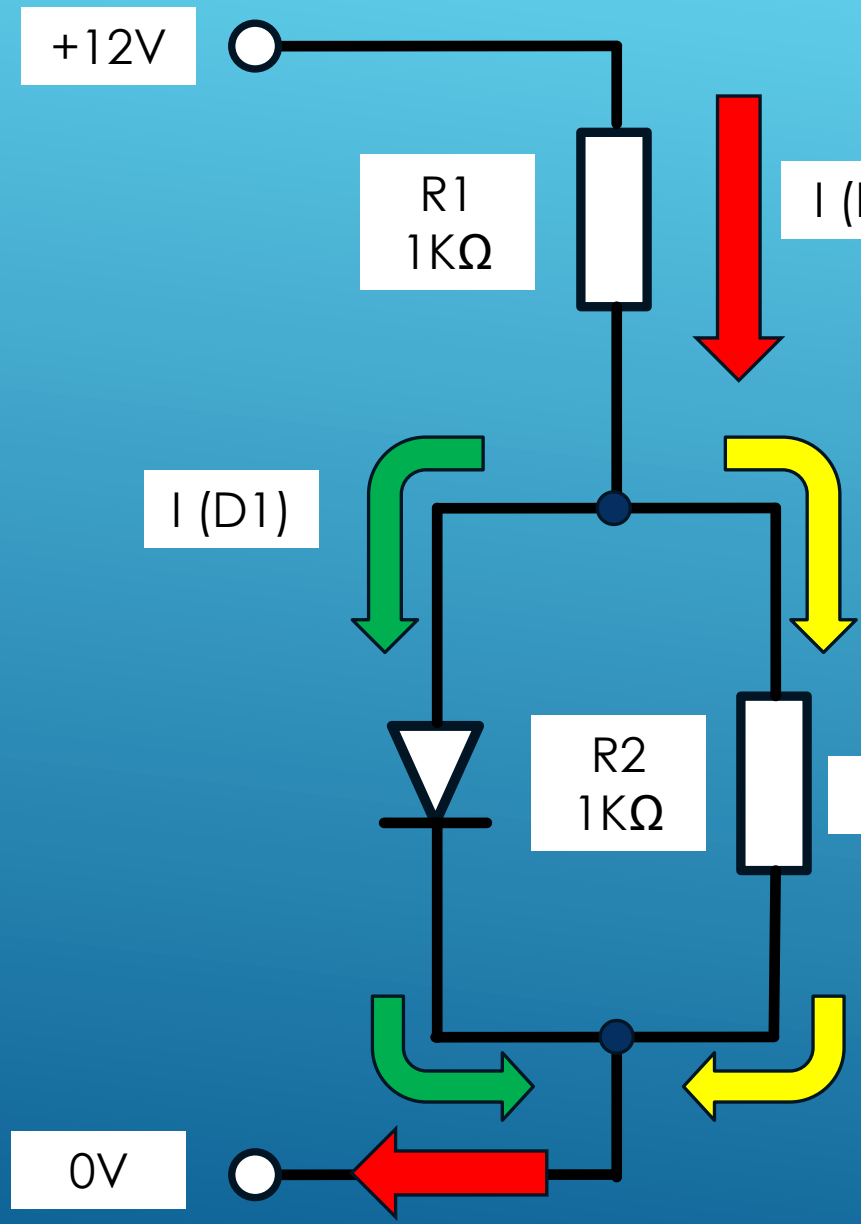
The DIODE D1 is FORWARD BIASED and CLAMPS the voltage across R2 at 0.7 Volts, IRRESPECTIVE of the current flowing through it

The voltage across R1 MUST therefore be CLAMPED at 12V – 0.7V = 11.3V
The diode clamp will not allow the voltage across R1 to change despite changes in current

The total current through R1 must be I = V/R or 11.3/1000 = 0.0113A or 11.3mA

Kirchhoff's First Law states the Current Arriving at a junction must equal the currents leaving a junction

STEP 2....



Kirchhoff's First Law states the Current Arriving at a junction must equal the sum of the currents leaving a junction

Apply OHM's LAW to the remaining LINEAR component (R2)

$I(R2) = V(R2)/R2$

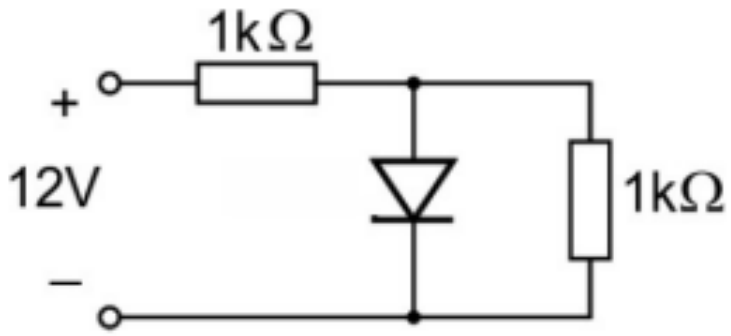
$I(R2) = 0.7/1000$

$I(R2) = 0.0007A$ or $0.7mA$

Since $I(R1) = I(D1) + I(R2)$ then
$I(D2) = I(R1) - I(R2) = 11.3mA - 0.7mA = 10.6mA$

BACK TO THE QUESTION ….

26. What current is flowing through the diode shown in the diagram?



A. 11.3mA.
B. 4.8mA.
C. 0mA
D. 10.6mA.

Remember the Hitchhikers Guide to the Galaxy!

DON'T PANIC!

It's EASY once you can spot the trick in the question!

IS THIS RELEVANT? OH YES! ……